REMARKS

The Final Office Action mailed on December 31, 2002, has been received and reviewed.

Claims 1-23 and 36-49 are currently pending in the above-referenced application. Each of claims 1-23 and 36-49 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-5, 10, 14-17, 36, 38, and 40 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,046,910 to Ghaem et al. (hereinafter "Ghaem").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Ghaem describes and illustrates a semiconductor device assembly 21 which includes a substrate 46 and an integrated circuit component 20 invertedly positioned over the substrate 46. The integrated circuit component 20 is a flip-chip type device with bond pads 26 arranged in an array on the active surface 22 thereof. A conductive adhesive 28 "flexibly" secures a conductive member 32 to each bond pad 26. Each conductive member 32 is also rigidly secured to a corresponding terminal 48 on a surface 70 of the substrate 46.

A polymeric body 50 substantially surrounds and is secured to the outer periphery of the integrated circuit component 20, as well as to surface 70 of the substrate 46. The polymeric body 50 serves to prevent moisture and contaminants from entering the space between the substrate 46 and the integrated circuit component 20.

The assembly 21 also includes one or more polymeric performs 40 positioned between the substrate 46 and the integrated circuit component 20. Each polymeric perform 40 is formed from "a compressible material which does not significantly interfere with the shrinkage of the polymeric bodies **50** during curing, cooling, or cross-linking." Col. 6, lines 13-19. The

polymeric performs 40 may be integrated into the packaging of the integrated circuit component 20 or affixed thereto (col. 6, lines 20-22), preferably before the integrated circuit component 20 is superimposed over the substrate 43 (col. 8, lines 31-36).

Independent claim 1 of the above-referenced application, as proposed to be amended, recites a method for modifying a semiconductor die. That method includes forming at least one stabilizer on an active surface of a semiconductor die or securing at least one stabilizer to the active surface of a semiconductor die. The at least one stabilizer is configured to space the at least one semiconductor die a substantially fixed distance apart from a higher-level substrate when the semiconductor die is disposed active surface-down of the higher-level substrate.

As the description of Ghaem is limited to polymeric performs 40 that are compressible, the polymeric performs 40 of Ghaem could not be configured to space the integrated circuit component 20 a fixed distance from the substrate 46 to which it is electrically connected. Moreover, Ghaem neither expressly nor inherently describes that the polymeric performs 40 thereof are useful for defining a substantially fixed distance between a semiconductor die and a substrate. Thus, Ghaem does not expressly or inherently describe a method which includes forming or securing spacers that are configured to "space . . . at least one semiconductor die a substantially fixed distance apart from a higher-level substrate," as recited in amended independent claim 1.

Therefore, it is respectfully submitted that Ghaem does not anticipate each and every element of amended independent claim 1, as is required to maintain a rejection under 35 U.S.C. § 102(b). As such, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 1 is allowable over Ghaem.

Claims 2-5, 10, and 14-17 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 5 is additionally allowable since Ghaem lacks any express or inherent description that the polymeric performs 40 thereof are formed "to have a height that defines a substantially consistent die-to-substrate distance". Instead, the polymeric performs 40 of Ghaem are

compressible, meaning that they would define variable die-to-substrate distance rather than a substantially consistent die-to-substrate distance.

Independent claim 36, as proposed to be amended, recites a method for electrically bonding a semiconductor device component to a substrate. The method of amended independent claim 36 includes, among other things, "forming at least one stabilizer structure comprising a dielectric material on at least one of [the] surface [of the semiconductor device component] and [the] substrate for disposal between [the] surface and [the] substrate."

As the description of Ghaem is limited to the placement of polymeric *performs* 40 to an integrated circuit component 20 or forming polymeric performs *in the packaging* of the integrated circuit component 20, it is respectfully submitted that Ghaem neither expressly nor inherently describes *forming* at least one stabilizer or one or both of a surface of a semiconductor device component and a substrate, as recited in amended independent claim 36.

Thus, Ghaem does not anticipate each and every element of amended independent claim 36. Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 36 is allowable over Ghaem.

Claims 38 and 40 are both allowable, among other reasons, as depending from claim 36, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 1-5, 10, 14-17, 36, 38, and 40 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Each of claims 6-9, 11-13, 18-23, 37, 39, and 41-49 stands rejected under 35 U.S.C. § 103(a).

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Ghaem

Claims 9, 11, and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem et al. (U.S. Patent No. 6,046,910) as applied to claims 1 through 5 above. Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 9, 11, and 12 are each allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Claim 11 is additionally allowable since Ghaem does not teach or suggest "applying a layer of insulative material on said active surface and patterning said layer." Instead, the teachings of Ghaem are limited to affixing polymeric performs 40 to the surface of an integrated circuit component 20 or forming them in the packaging of the integrated circuit component (col. 6, lines 20-22), neither of which qualifies as "patterning [a] layer" of insulative material.

Claim 12 is also allowable because Ghaem neither teaches nor suggests "applying a layer of photoresist material on said active surface and patterning said layer."

Ghaem in View of Juskey and Hull

Claims 6, 7, 18, 19, 23, 41-45, and 47-49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem and, further, in view of U.S. Patent 5,264,061 to Juskey et al. (hereinafter "Juskey") and U.S. Patent 4,575,330 to Hull (hereinafter "Hull").

Claims 6 and 7 are both allowable, among other reasons, as depending either directly or indirectly from claim 1, which is allowable.

Independent claim 18 recites a method of fabricating a semiconductor device component that includes, among other things, sequentially forming a plurality of superimposed, contiguous, mutually adhered photopolymer layers of at least one stabilizer on a surface of a semiconductor device component.

Independent claim 19 is drawn to a method of fabricating a semiconductor device component that includes placing at least one semiconductor substrate having an active surface with contact pads exposed thereon in a horizontal plane, recognizing a location and orientation of the at least one substrate, and stereolithographically forming on the active surface at least one stabilizer comprising at least one layer of an electrically nonconductive semisolid material.

Independent claim 41, as amended and presented herein, is directed to a method of modifying a semiconductor die. The method of amended independent claim 41 includes, among other things, applying a layer of a partially uncured photopolymer to a semiconductor die and stereolithographically forming at least one stabilizer on the semiconductor die.

It is respectfully submitted that a *prima facie* case of obviousness cannot be made against independent claims 18, 19 and 41 based upon the asserted combination of Ghaem, Juskey, and Hull.

Juskey teaches a method of making a three-dimensional printed circuit assembly by forming successive adjacent layers of an object using stereolithography. *See* col. 1, lines 54-63; col. 2, lines 30-52. A substrate is first formed from a photoactive polymer that is capable of altering its physical state when exposed to a radiant beam. At this point, the substrate is only partially cured. A conductive circuit pattern is formed on the partially cured substrate and the

substrate is then molded to create a three-dimensional structure. The substrate is then further cured to cause the photoactive polymer to harden completely.

Hull teaches an apparatus for stereolithographically fabricating three dimensional objects. The teachings of Hull are directed to simplified means for rapid prototyping of parts to allow quickly and economically moving from a design stage to production. *See* col. 1, line 63, to col. 2, line 12.

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Ghaem, Juskey, and Hull in the manner that has been asserted. In particular, while the teachings of Ghaem are not specific as to the manner in which the polymeric performs 40 thereof are formed, there is no teaching in either Juskey or Hull that the equipment and processes described therein may be used to fabricate one or more stabilizers *on semiconductor dice.* The teachings of Juskey and Hull that the processes thereof are useful with microelectronics and electronic printed circuit design (*see* Final Office Action, page 7) do not amount to a teaching, suggestion, or motivation that these processes would be useful for forming one or more stabilizers on semiconductor dice.

Therefore, it appears that the only motivation to combine the teachings of Ghaem, Juskey, and Hull in the manner that has been asserted could only have been improperly gleaned from the hindsight provided by the specification of the above-referenced application.

Second, with respect to independent claim 19, it is respectfully submitted that none of Ghaem, Juskey, or Hull teaches or suggests "recognizing a location and orientation of . . . at least one substrate."

For these reasons, it is respectfully submitted that the teachings of Ghaem, Juskey, and Hull do not support a *prima facie* case of obviousness against any of independent claims 18, 19, and 41, as is required to maintain a rejection under 35 U.S.C. § 103(a). Therefore, it is respectfully submitted that, under 35 U.S.C. § 103(a), each of independent claims 18, 19, and 41 is allowable over Ghaem, Juskey, and Hull, taken either separately or together.

Claim 23 is allowable, among other reasons, as depending indirectly from claim 19, which is allowable.

Claims 42-45 and 47-49 are each allowable, among other reasons, as depending either directly or indirectly from claim 41, which is allowable.

Ghaem in View of Juskey and Hull and, Further, in View of Migdal

Claims 20-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem, in view of Juskey and Hull and, further, in view of U.S. Patent 5,870,220 to Migdal (hereinafter "Migdal").

Claims 20-22 are each allowable, among other reasons, as depending either directly or indirectly from claim 19, which is allowable.

Moreover, Migdal does not include any teaching or suggestion that remedies the shortcomings of Ghaem, Juskey, and Hull with respect to the use of stereolithographic processes to form one or more stabilizers on semiconductor dice.

Therefore, it is respectfully submitted that there would have been no motivation to one of ordinary skill in the art to combine the teachings of Ghaem, Juskey, Hull, and Migdal in the manner that has been asserted and, thus, that a *prima facie* case has not been established against any of claims 20-22. It is, therefore, respectfully submitted that, under 35 U.S.C. § 103(a), each of claims 20-22 is allowable over Ghaem, Juskey, Hull, and Migdal, taken either separately or together.

Ghaem in View of Juskey and Hull and, Further, in View of Kuniaki

Claims 8, 13, and 46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem et al. (U.S. Patent No. 6,046,910) in view of Juskey et al. (U.S. Patent No. 5,264,061) and Hull (U.S. Patent No. 4,575,330), as applied to claims 1, 18, 19, and 41 above, and further in view of Kuniaki (Japanese Patent No. JP10189653). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 8 and 13 are both allowable, among other reasons, as depending from claim 1, which is allowable.

Claim 46 is allowable, among other reasons, as depending from claim 41, which is allowable.

In addition, each of claims 8, 13, and 46 is allowable since one of ordinary skill in the art would not have been motivated to combine the teachings of these references. In particular, Kuniaki, which is relied for its teaching that an underfill material may be introduced in the space between a flip-chip or grid array type semiconductor device and a carrier substrate therefore, does not include any teaching or suggestion that would remedy the aforementioned deficiencies of Ghaem, Juskey, and Hull with respect to motivating one of ordinary skill in the art to use stereolithographic processes to form stabilizers on semiconductor dice.

Moreover, it is respectfully submitted that, by teaching the introduction of an underfill material between a semiconductor device and a carrier substrate, Kuniaki teaches away from the subject matter of Ghaem. In particular, Kuniaki teaches away from the use of polymeric bodies 50 that expressly do not extend between an integrated circuit component 20 and a substrate 46 to avoid problems that are associated with the use of underfill materials.

Accordingly, it is respectfully submitted that a *prima facie* case of obviousness has not been established against any of claims 8, 13, and 46 and, thus, that, under 35 U.S.C. § 103(a), each of these claims is allowable over Ghaem, Juskey, Hull, and Kuniaki, taken either separately or together.

Ghaem in View of Lin

Claims 37 and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem, in view of U.S. Patent 3,871,015 to Lin et al. (hereinafter "Lin").

Claims 37 and 39 are both allowable, among other reasons, as depending from claim 36, which is allowable.

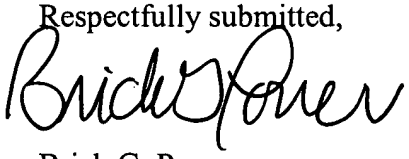
ENTRY OF AMENDMENTS

It is respectfully submitted that the claim amendments that have been proposed herein should be entered since they are supported by the as-filed specification and, thus, do not introduce new matter into the above-referenced application and since they would not require an additional search or otherwise raise new issues. If, for some reason, it is determined that the proposed amendments do not place the above-referenced application in condition for allowance, entry thereof is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

It is respectfully submitted that each of claims 1-23 and 36-49 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicant(s)
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: February 28, 2003

Enclosure: Version With Markings to Show Changes Made

BGP/ps:djp
Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE:

Please amend the title as follows:

STEREOLITHOGRAPHIC METHOD FOR FABRICATING STABILIZERS FOR [FLIP-CHIP TYPE] SEMICONDUCTOR DEVICES

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended four times) A method of [forming] modifying a [flip-chip] semiconductor die, comprising:

providing at least one [flip-chip] semiconductor die having an active surface; and

forming on or securing to said active surface at least one stabilizer comprising a dielectric material [and securing said at least one stabilizer to said active surface so as to protrude] such that said at least one stabilizer protrudes from said active surface, said at least one stabilizer being configured to [at least partially stabilize an orientation of] space said at least one [flip-chip] semiconductor die a substantially fixed distance apart from a higher-level substrate when disposed [face] active surface-down over [a] said higher-level substrate.

8. (Amended) The method of claim 1, wherein said providing comprises providing at least one [flip-chip] semiconductor die having a sealing material on an active surface thereof and wherein said forming comprises forming said at least one stabilizer to be securable to said sealing material.

9. (Amended) The method of claim 1, wherein said providing comprises providing a semiconductor wafer including a plurality of [flip-chip] semiconductor dice.

13. (Twice amended) The method of claim 1, further comprising introducing an encapsulant material between said at least one [flip-chip] semiconductor die and said substrate.

15. (Amended) The method of claim 1, further comprising disposing at least one conductive structure on at least one bond pad of said at least one [flip-chip] semiconductor die.

18. (Amended four times) A method of [fabricating] modifying a semiconductor device component, comprising:

providing at least one semiconductor substrate with contact pads on an active surface thereof; and

sequentially forming on said active surface at least one stabilizer having a plurality of superimposed, contiguous, mutually adhered layers of photopolymer, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device component upon being disposed [face] active surface-down over a higher-level substrate.

19. (Amended four times) A method of [fabricating] modifying a semiconductor device component, comprising:

placing at least one semiconductor substrate having an active surface with contact pads exposed thereon in a horizontal plane;

recognizing a location and orientation of said at least one substrate;

stereolithographically forming on said active surface, between one of said contact pads and a peripheral edge of said at least one substrate, at least one stabilizer comprising at least one layer of an electrically nonconductive semisolid material.

36. (Amended four times) A method for electrically bonding a [flip-chip] semiconductor device component having a surface and conductive structures protruding from said surface to a substrate having contacts positioned correspondingly to said conductive structures, said method comprising:

forming at least one stabilizer structure comprising a dielectric material [configured to be disposed] on at least one of said surface and said substrate for disposal between said surface and said substrate;

inverting and positioning said semiconductor device component on said substrate to contact said conductive structures to corresponding contacts; and

bonding said conductive structures to the corresponding contacts.

41. (Twice amended) A method of [forming] modifying a [flip-chip] semiconductor die, comprising:

providing at least one [flip-chip] semiconductor die having an active surface with contact pads exposed thereon;

applying a layer of a partially uncured photopolymer to said [flip-chip] semiconductor; and

stereolithographically forming on said [flip-chip] semiconductor, between one of said contact pads and a peripheral edge of said [flip-chip] semiconductor, at least one stabilizer securable to said active surface so as to protrude from said active surface, said at least one stabilizer being a structure configured to at least partially stabilize an orientation of said at least one [flip-chip] semiconductor die when disposed [face] active surface-down over a higher-level substrate.

45. (Amended) The method of claim 41, wherein said providing comprises providing a semiconductor wafer including a plurality of [flip-chip] semiconductor dice.

46. (Amended) The method of claim 41, further comprising introducing an encapsulant material between said at least one [flip-chip] semiconductor die and said substrate.

48. (Amended) The method of claim 41, further comprising disposing at least one conductive structure on at least one bond pad of said at least one [flip-chip] semiconductor die.